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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,502	01/27/2004	Mutsumi Kimura	118215	9268

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,502	KIMURA ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *1-4 and 7-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5, 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda et al. ("Surface Free Technology by Laser Annealing (SUFTLA)", IEEE, 1999), hereafter Shimoda[1], in view of Shimoda et al. ("Future Trend of TFT Technology", AM-LCD 2002), hereafter Shimoda[2] and JP 2003-297974-A.

Shimoda[1] teaches a method of manufacturing thin film transistors in figures 1 and 2, for example. Shimoda[1] teach:

- forming functional elements (TFT's) in a predetermined shape (formed as TFT's) on a first substrate (original substrate) via a peeling layer (exfoliation layer) which causes peeling by application of a predetermined amount of energy (XeCl laser irradiation); and
- transferring at least one of the functional elements (TFT's) directly to a second substrate (1st transfer substrate) by applying the energy (XeCl laser irradiation) to relevant portions of the peeling layer (exfoliation layer) corresponding to regions of the functional elements to cause peeling.

Shimoda[1] does not teach forming the functional elements using holographic lithography to pattern the functional elements.

Shimoda[2] teaches future trends in TFT technology. On page 7, first paragraph below the figure, Shimoda[2] teach forming TFT's using a new holography photolithography (holographic lithography) which allows patterns as small as 0.5 micron.

Shimoda[1] and Shimoda[2] are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the holographic lithography of Shimoda[2] in patterning the TFT's of Shimoda[1]. The motivation for doing so is to reduce the size of the TFT's to obtain high performance TFT's.

Shimoda[1] and Shimoda[2] do not teach the second substrate containing a wiring line, the transfer including electrically connecting the at least one functional element to the wiring line of the second substrate.

JP 2003-297974-A teach in figure 1(a) and 1(b) a method of manufacturing thin film elements including transferring elements 13 from a first substrate 11 to a second substrate 14 where the second substrate includes a wiring line 17/18 and the functional elements 13 are electrically connected to the wiring line of the second substrate.

Shimoda[1] with Shimoda[2] and JP 2003-297974-A are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a wiring line on the second substrate and electically connect the functional element to the wiring line. The motivation for doing so is to allow a large number of varying semiconductor devices to be integrated onto a printed circuit board which allows electrical connection between the different devices and chips and connection to a variety of peripheral components.

With regard to claim 6, the thin film functional elements of Shimoda[1] are thin film transistors (TFT's).

With regard to claim 10, in the combination of references, using the holographic lithography and the desired reduction in TFT size, it would have been obvious to use a design rule of 1.0 micron or less to pattern the functional elements.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoda et al. ("Surface Free Technology by Laser Annealing (SUFTLA)", IEEE, 1999), hereafter Shimoda[1], in view of Applicants Admitted Prior Art, hereafter APA and JP 2003-297974-A.

Shimoda[1] teaches a method of manufacturing thin film transistors in figures 1 and 2, for example. Shimoda[1] teach:

- forming functional elements (TFT's) in a predetermined shape (formed as TFT's) on a first substrate (original substrate) via a peeling layer (exfoliation layer) which causes peeling by application of a predetermined amount of energy (XeCl laser irradiation); and
- transferring at least one of the functional elements (TFT's) directly to a second substrate (1st transfer substrate) by applying the energy (XeCl laser irradiation) to relevant portions of the peeling layer (exfoliation layer) corresponding to regions of the functional elements to cause peeling.

Shimoda[1] does not teach forming the functional elements using dynamic auto focus to pattern the functional elements.

APA teach in paragraph [0008] that dynamic auto focus is known in forming thin film transistors.

Shimoda[1] and APA are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the dynamic auto focus of APA in patterning the TFT's of Shimoda[1]. The motivation for doing so is so that surface swelling of large substrates can be compensated for.

Shimoda[1] and APA do not teach the second substrate containing a wiring line, the transfer including electrically connecting the at least one functional element to the wiring line of the second substrate.

JP 2003-297974-A teach in figure 1(a) and 1(b) a method of manufacturing thin film elements including transferring elements 13 from a first substrate 11 to a second substrate 14 where the second substrate includes a wiring line 17/18 and the functional elements 13 are electrically connected to the wiring line of the second substrate.

Shimoda[1] with APA and JP 2003-297974-A are combinable because they are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to include a wiring line on the second substrate and electically connect the functional element to the wiring line. The motivation for doing so is to allow a large number of varying semiconductor devices to be integrated

onto a printed circuit board which allows electrical connection between the different devices and chips and connection to a variety of peripheral components.

Response to Arguments

4. Applicant's arguments with respect to claims 5, 6, 10 and 11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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